25 Spring ECEN 720: High-Speed Links: Circuits and Systems Pre-lab Report

Lab6: Link Modeling with ADS

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1. In digital circuit design, there are many switching signals. Finite supply impedance causes switching output noise. Build the circuit shown in Figure 28 with supply inductance and decoupling capacitance. Use Case 1: CLK (i.e. 1010 pattern) and Case 2: 7-bits PRBS as the input sources. CLK frequency is set to be 2.5GHz with 20ps rise/fall time. PRBS date rate is 5Gb/s with 20ps rise/fall time. Please plot the output eye diagrams. Compare the results with the case having ideal supply (zero supply impedance by removing all parasitics).

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